



浙江芯芯电子有限公司
ZHEJIANG XINXIN ELECTRICAL CO., LTD.

产品规格书

Specification of Products

产品名称：平板型

产品型号：KP2500A

浙江芯芯电子有限公司

ZHEJIANG XINXIN ELECTRICAL CO., LTD.

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Features

- Center amplifying gate
- Metal case with ceramic insulator
- Low on-state and switching losses

Typical Applications

- AC controllers
- DC and AC motor control
- Controlled rectifiers

$I_{T(AV)}$ 2670 A
 V_{DRM}/V_{RRM} 1100-1800V
 I_{TSM} 38 kA
 I^2t 7220 $10^3 A^2S$



SYMBOL	CHARACTERISTIC	TEST CONDITIONS	$T_j(^\circ C)$	VALUE			UNIT
				Min	Type	Max	
$I_{T(AV)}$	Mean on-state current	180° half sine wave 50Hz Double side cooled,	125			3110	A
						2670	
V_{DRM} V_{RRM}	Repetitive peak off-state voltage Repetitive peak reverse voltage	$V_{DRM} \& V_{RRM}$ tp=10ms $V_{DSM} \& V_{RSM} = V_{DRM} \& V_{RRM} + 100V$	125	1100		1800	V
I_{DRM} I_{RRM}	Repetitive peak current	$V_{DM} = V_{DRM}$ $V_{RM} = V_{RRM}$	125			160	mA
I_{TSM}	Surge on-state current	10ms half sine wave $V_R=0.6V_{RRM}$	125			38	kA
I^2t	I^2T for fusing coordination					7220	$A^2s * 10^3$
V_{TO}	Threshold voltage		125			0.80	V
r_T	On-state slop resistance					0.14	$m\Omega$
V_{TM}	Peak on-state voltage	$I_{TM}=5000A, F=35kN$	125			1.50	V
dv/dt	Critical rate of rise of off-state voltage	$V_{DM}=0.67V_{DRM}$	125			1000	$V/\mu s$
di/dt	Critical rate of rise of on-state current	$V_{DM}=67\%V_{DRM}$ to 3000A, Gate pulse $t_r \leq 0.5\mu s$ $I_{GM}=1.5A$	125			250	$A/\mu s$
Q_{rr}	Recovery charge	$I_{TM}=2000A, tp=2000\mu s, di/dt=-20A/\mu s, V_R=50V$	125		2000		μC
I_{GT}	Gate trigger current	$V_A=12V, I_A=1A$	25	40		300	mA
V_{GT}	Gate trigger voltage			0.8		3.0	V
I_H	Holding current			20		300	mA
V_{GD}	Non-trigger gate voltage	$V_{DM}=67\%V_{DRM}$	125	0.3			V
$R_{th(j-c)}$	Thermal resistance Junction to case	At 180° sine double side cooled Clamping force 35.0kN				0.012	$^\circ C / W$
$R_{th(c-h)}$	Thermal resistance case to heatsink					0.003	
F_m	Mounting force			30		40	kN
T_{stg}	Stored temperature			-40		140	$^\circ C$
W_t	Weight				880		g
Outline		KT60cT70					

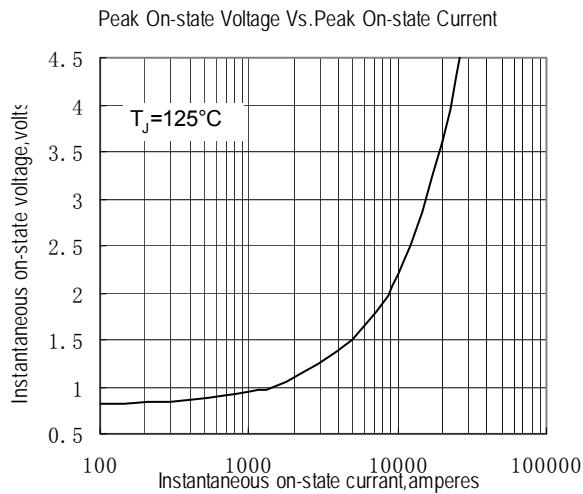


Fig.1

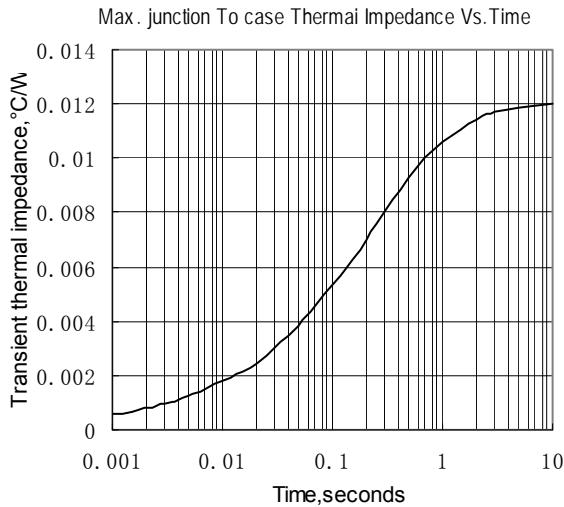


Fig.2

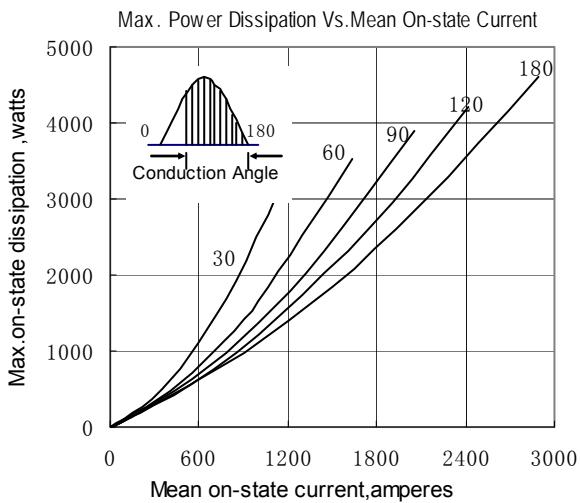


Fig.3

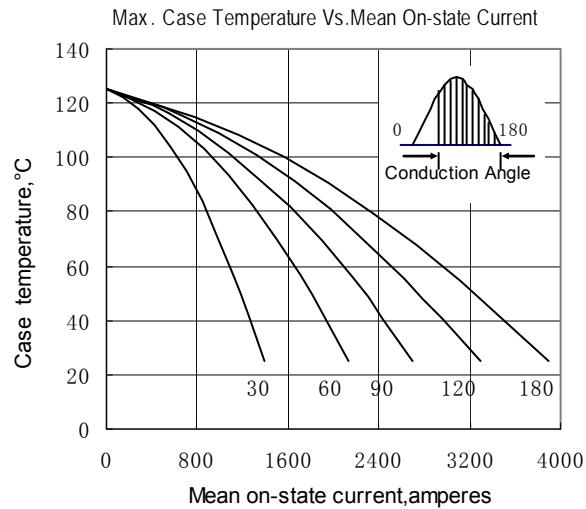


Fig.4

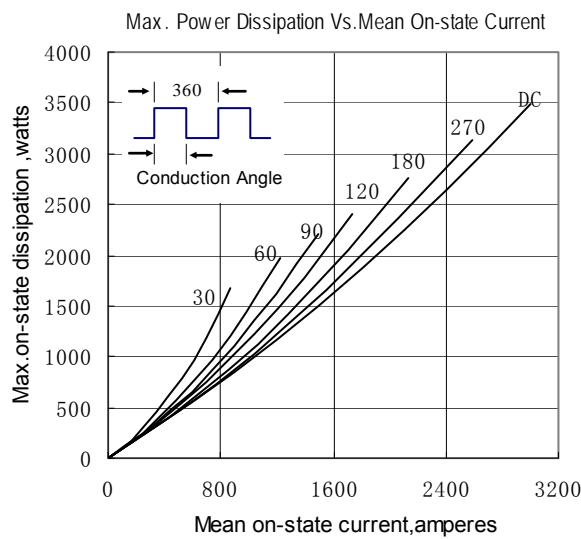


Fig.5

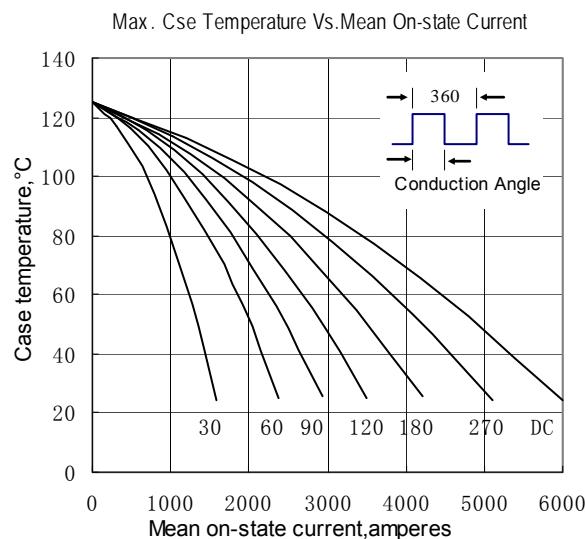


Fig.6

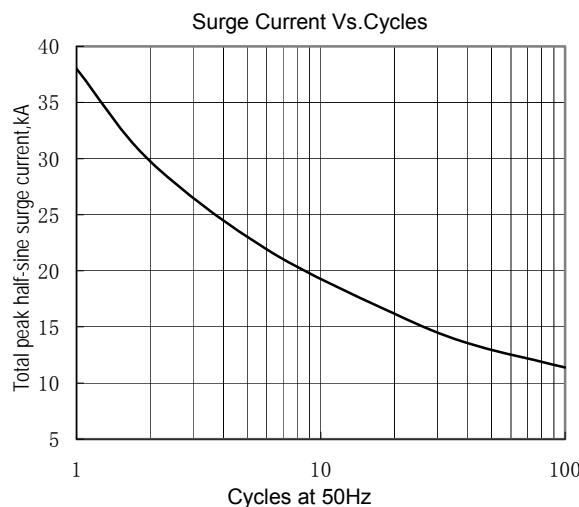


Fig.7

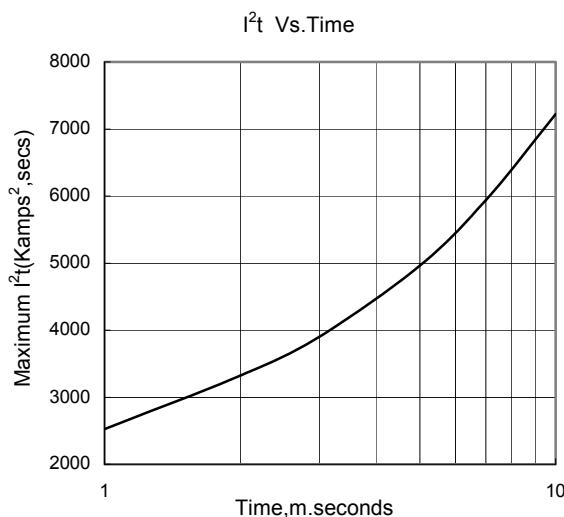


Fig.8

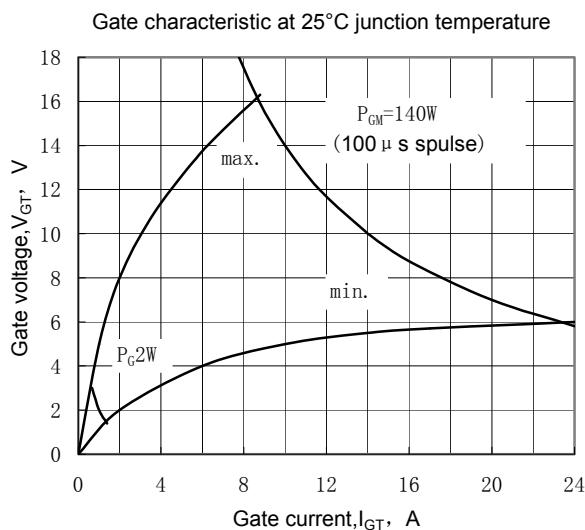


Fig.9

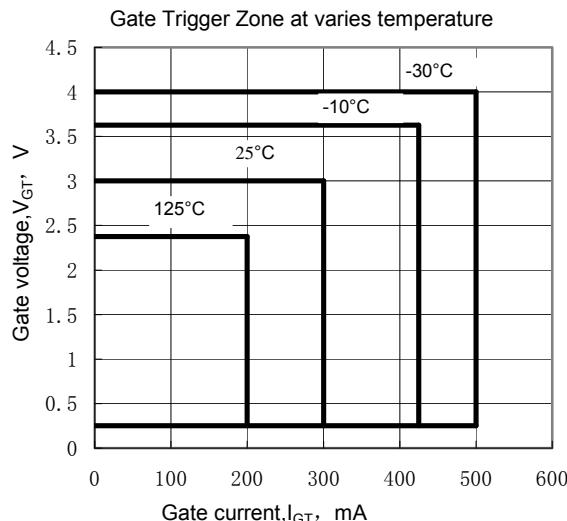


Fig.10

Outline:

