



浙江芯芯电子有限公司
ZHEJIANG XINXIN ELECTRICAL CO., LTD.

产品规格书

Specification of Products

产品名称：平板型

产品型号：KP5000A

浙江芯芯电子有限公司

ZHEJIANG XINXIN ELECTRICAL CO., LTD.

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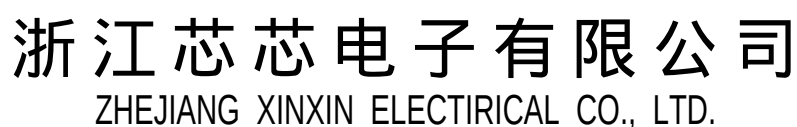
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拟制	审核	核准
丁国盛	李园利	麻伟阳

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- Center amplifying gate
- Metal case with ceramic insulator
- Low on-state and switching losses

- AC controllers
- DC and AC motor control
- Controlled rectifiers

$I_{T(AV)}$	5010	A
V_{DRM}/V_{RRM}	4500-5500	V
I_{TSM}	72	kA
I^2t	25920	$10^3 A^2S$



SYMBOL	CHARACTERISTIC	TEST CONDITIONS		T _J (°C)	VALUE			UNIT
					Min	Type	Max	
I _{T(AV)}	Mean on-state current	180° half sine wave 50Hz Double side cooled,	T _C =55°C	125			5800	A
			T _C =70°C				5010	
V _{DRM} V _{RRM}	Repetitive peak off-state voltage Repetitive peak reverse voltage	V _{DRM} &V _{RRM} tp=10ms V _{DSM} &V _{RSM} = V _{DRM} &V _{RRM} +100V		125	4500		5500	V
I _{DRM} I _{RRM}	Repetitive peak current	V _{DM} = V _{DRM} V _{RM} = V _{RRM}		125			600	mA
I _{TSM}	Surge on-state current	10ms half sine wave		125			72	kA
I ² t	I ² T for fusing coordination	V _R =0.6V _{RRM}					25920	A ² s*10 ³
V _{TO}	Threshold voltage			125			1.02	V
r _T	On-state slop resistance						0.14	mΩ
V _{TM}	Peak on-state voltage	I _{TM} =3000A, F=120kN		125			1.50	V
dv/dt	Critical rate of rise of off-state voltage	V _{DM} =0.67V _{DRM}		125			2000	V/μs
di/dt	Critical rate of rise of on-state current	V _{DM} = 67%V _{DRM} to 3000A, Gate pulse tr ≤0.5μs IGM=1.5A		125			250	A/μs
Q _{rr}	Recovery charge	I _{TM} =2000A,tp=2000μs, di/dt=-5A/μs, V _R =50V		125		5500		μC
I _{GT}	Gate trigger current	VA=12V, IA=1A		25	40		300	mA
V _{GT}	Gate trigger voltage				0.8		3.0	V
I _H	Holding current				25		250	mA
V _{GD}	Non-trigger gate voltage	V _{DM} =67%V _{DRM}		125	0.3			V
R _{th(j-c)}	Thermal resistance Junction tocase	At 180° sine double side cooled Clamping force 120.0kN					0.004	°C /W
R _{th(c-hs)}	Thermal resistance case to heatsink						0.001	°C /W
F _m	Mounting force				110	120	140	kN
T _{stg}	Stored temperature				-40		140	°C
W _t	Weight					3420		g
Outline	KT110dT							

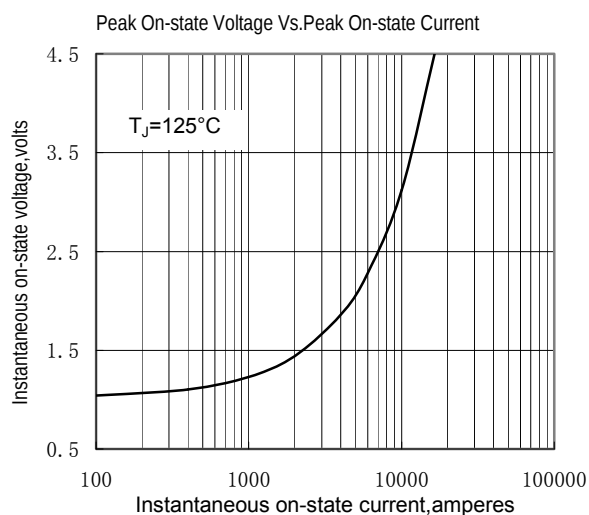


Fig.1

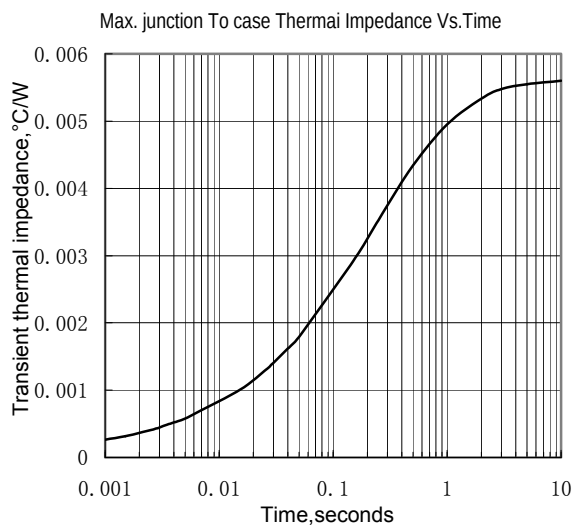


Fig.2

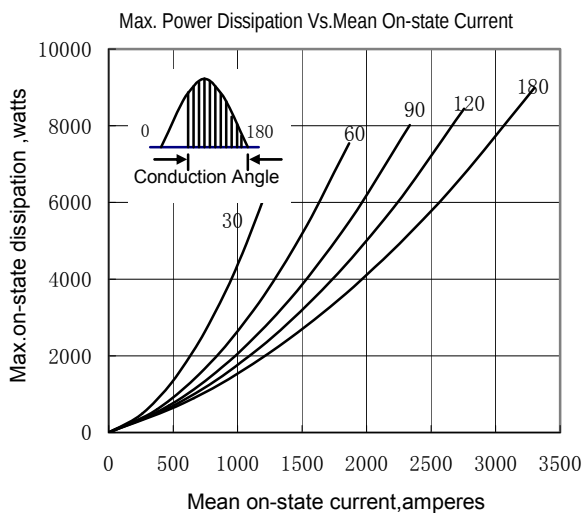


Fig.3

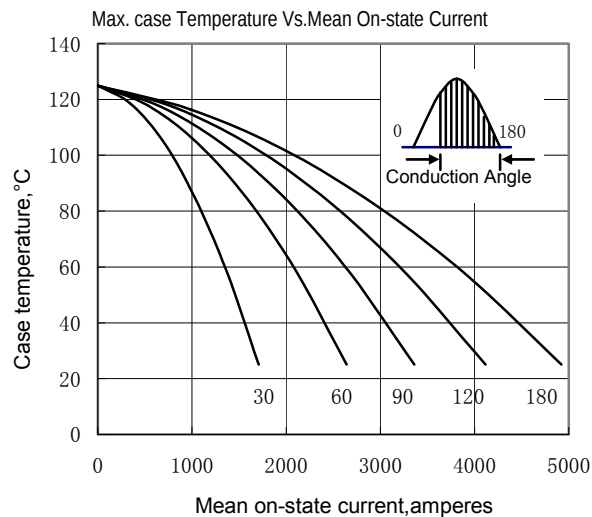


Fig.4

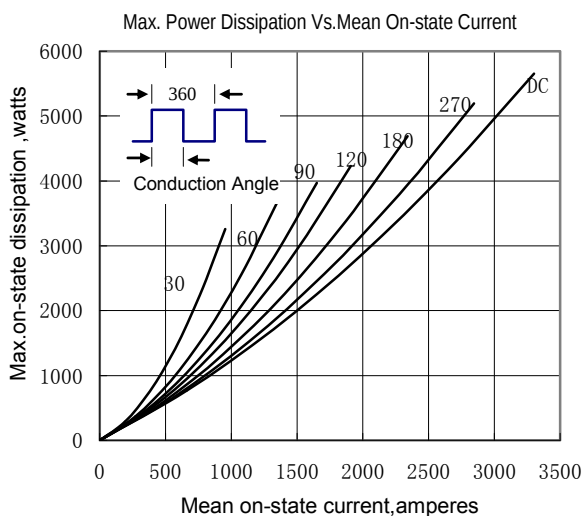


Fig.5

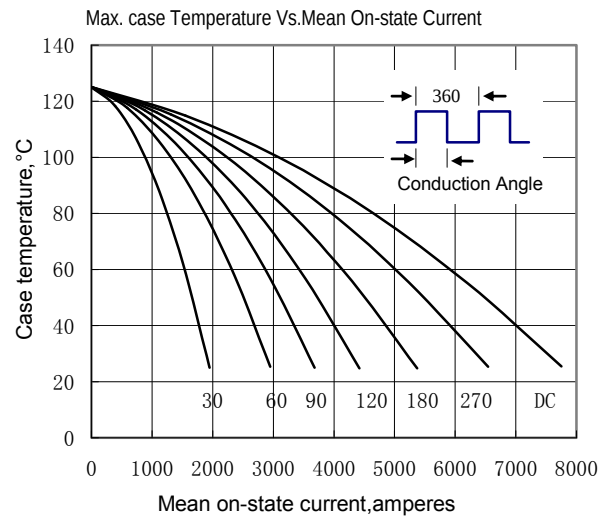


Fig.6

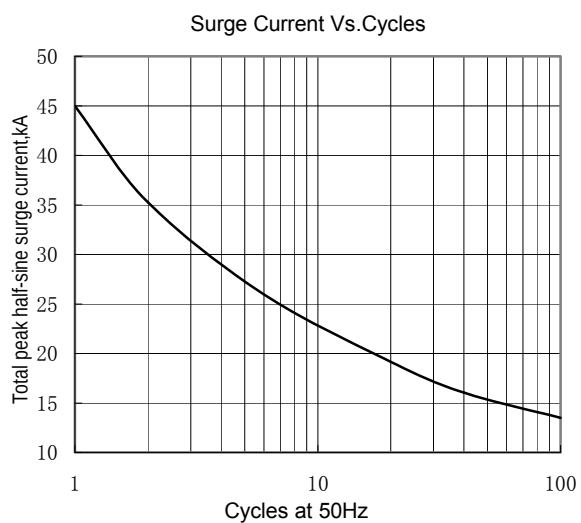


Fig.7

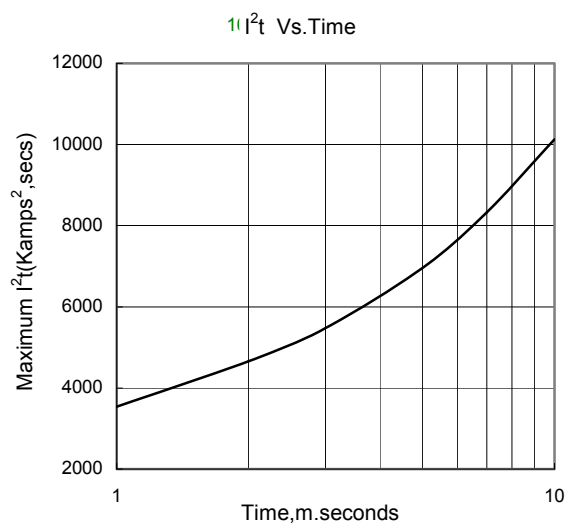


Fig.8

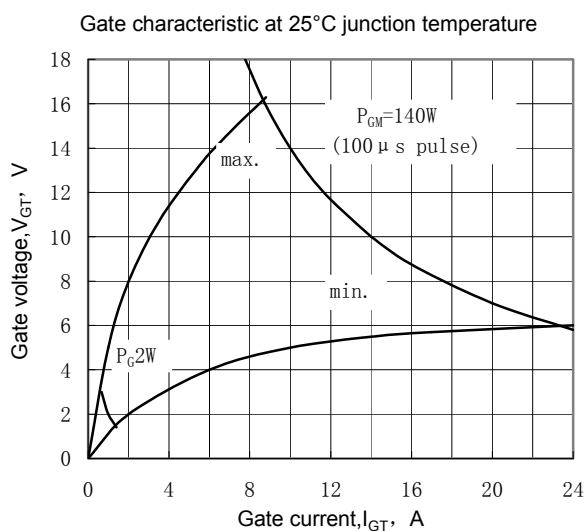


Fig.9

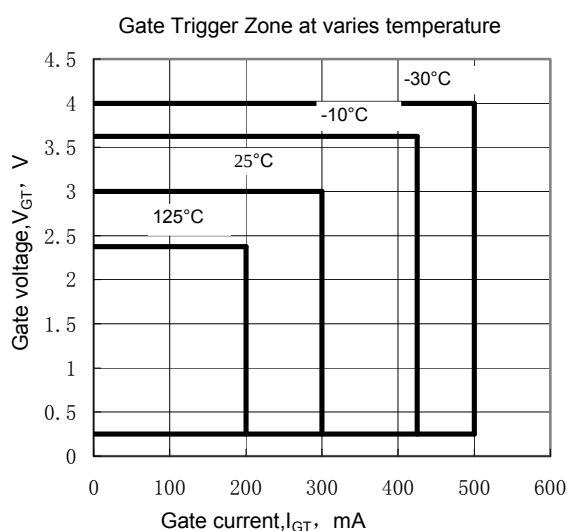


Fig.10

Outline:

