



浙江芯芯电子有限公司
ZHEJIANG XINXIN ELECTIRICAL CO., LTD.

产品规格书

Specification of Products

产品名称：可控硅模块

产品型号：MFC70A

浙江芯芯电子有限公司

ZHEJIANG XINXIN ELECTIRICAL CO., LTD.

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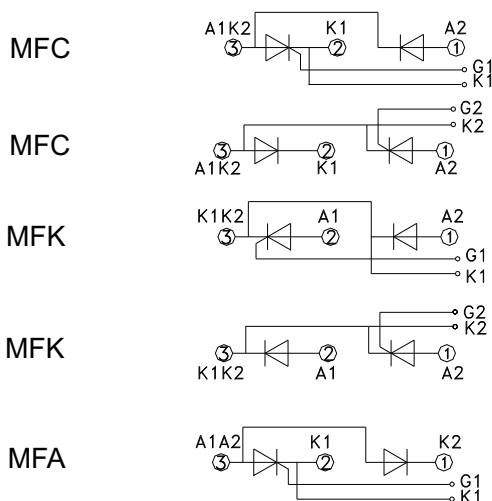
<http://www.zjxxdz1.com>

拟制	审核	核准
丁国盛	李园利	麻伟阳

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SYMBOL	CHARACTERISTIC	TEST CONDITIONS	T _j (°C)	VALUE			UNIT
				Min	Type	Max	
I _{T(AV)} I _{F(AV)}	Mean on-state current	180° half sine wave 50Hz Single side cooled, T _j =85°C	125			70	A
I _{T(RMS)}	RMS on-state current	Single side cooled, T _j =85°C	125			110	A
V _{DRM} V _{RRM}	Repetitive peak on-state voltage Repetitive peak reverse voltage	V _{DRM} &V _{RRM} tp=10ms V _{DsM} &V _{RSM} = V _{DRM} &V _{RRM} +200V respectively	125	600		1800	V
I _{DRM} I _{RRM}	Repetitive peak current	at V _{DRM} at V _{RRM}	125			10	mA
I _{TSM}	Surge on-state current	10ms half sinewave	125			1.60	KA
I ² t	I ² T for fusing coordination	V _R =60%V _{RRM}				13.0	A ² s*10 ³
V _{TO}	Threshold voltage		125			0.80	V
r _T	On-state slop resistance					2.64	mΩ
V _{TM}	Peak on-state voltage	I _{TM} =210A	125			1.4	V
dv/dt	Critical rate of rise of off-state voltage	V _{DM} =67%V _{DRM}	125			800	V/μs
di/dt	Critical rate of rise of on-state current	From 67%V _{DRM} to 210A, Gate source 1.5A t _r ≤ 0.5 μs Repetitive	125			50	A/μs
I _{GT}	Gate trigger current			20		100	mA
V _{GT}	Gate trigger voltage	V _A =12V, I _A =1A	25	0.7		2.0	V
I _H	Holding current			20		100	mA
V _{GD}	Non-trigger gate voltage	At 67%V _{DRM}	125			0.2	V
R _{th(j-c)}	Thermal resistance Junction to heatsink	At 180° sine Single side cooled				0.410	°C /W
V _{iso}	Isolation voltage	50Hz, RM. S, t=1min, i _{so} : 1mA MAX)		2500			V
F _m	Thermal connection torque(M5)					0.20	N.m
	Mounting torque(M6)					0.30	N.m
T _{stg}	Stored temperature			-40		140	°C
W _i	Weight					154	g
Outline							

OUTLINE DRAWING & CIRCUIT DIAGRAM



Rating and Characteristic

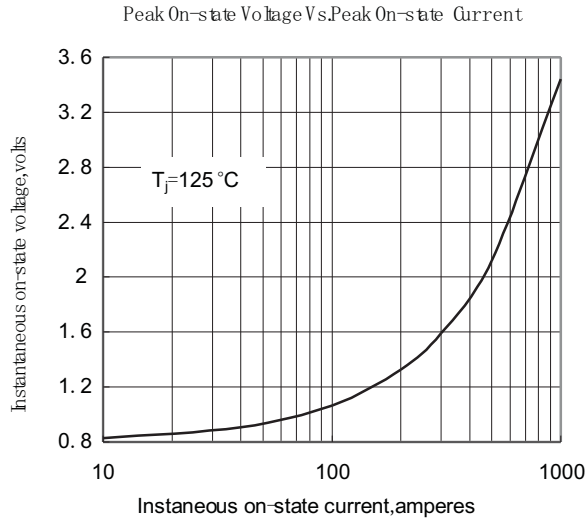


Fig. 1

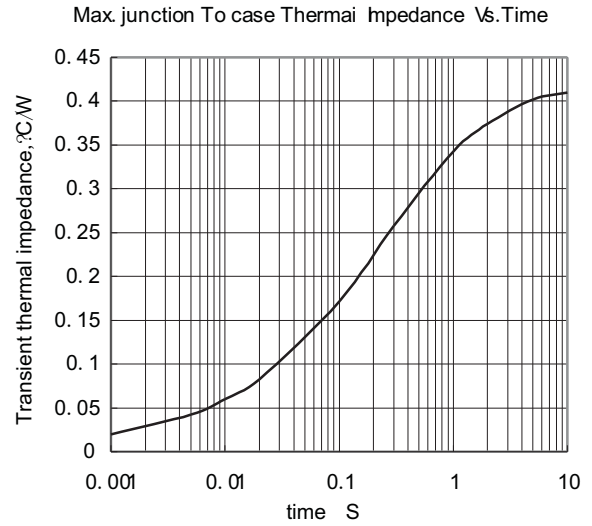


Fig. 2

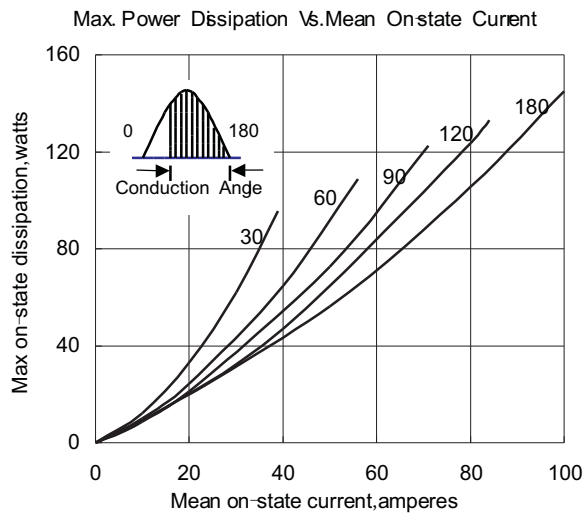


Fig. 3

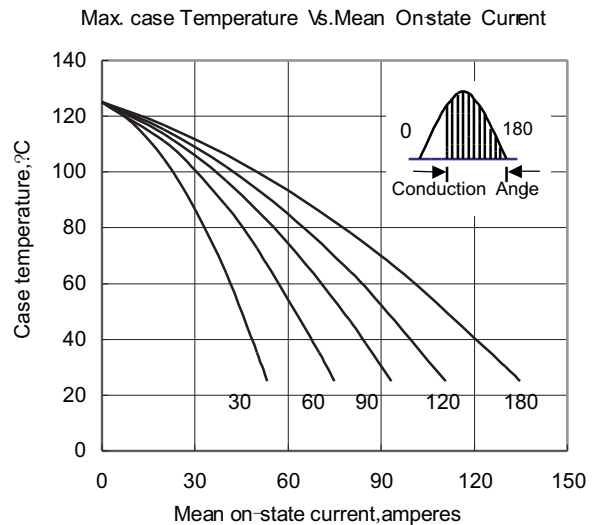


Fig. 4

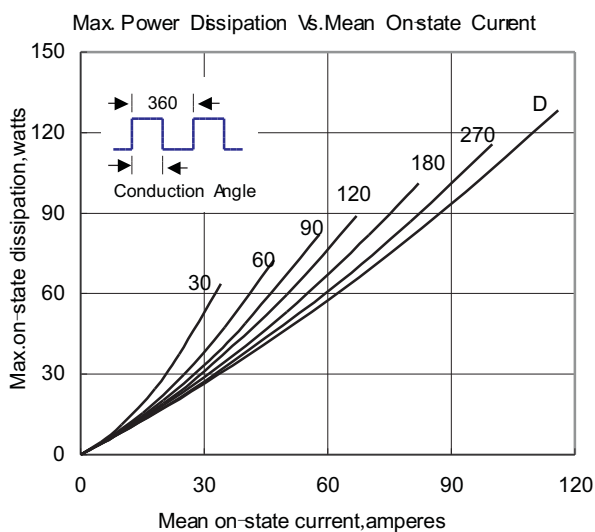


Fig. 5

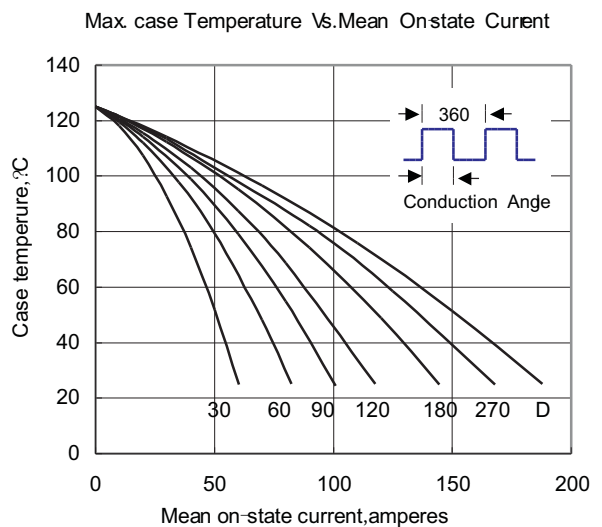


Fig. 6

Rating and Characteristic

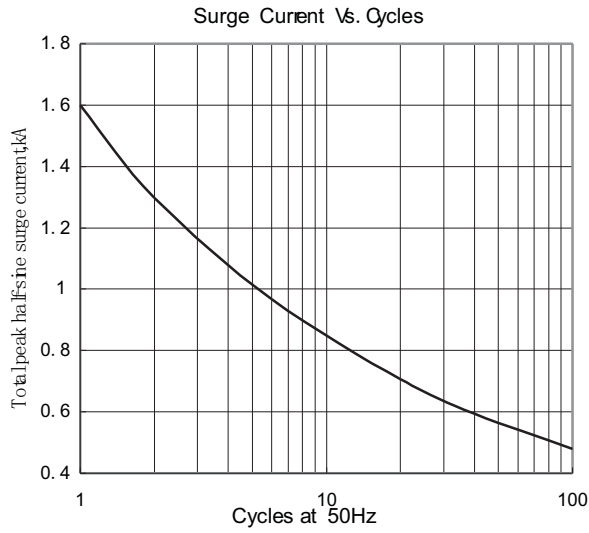


Fig. 7

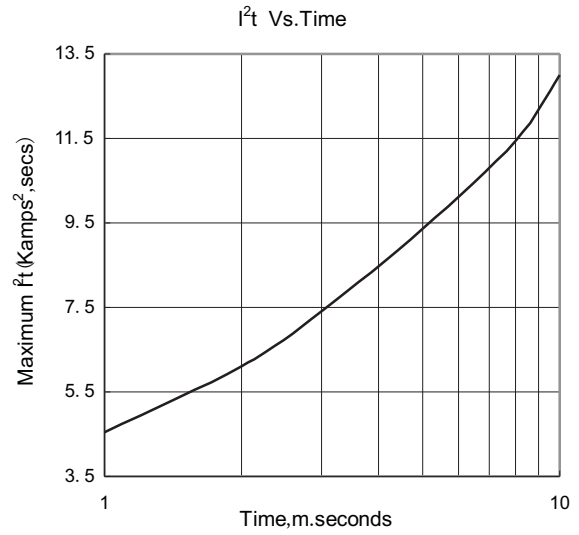


Fig. 8

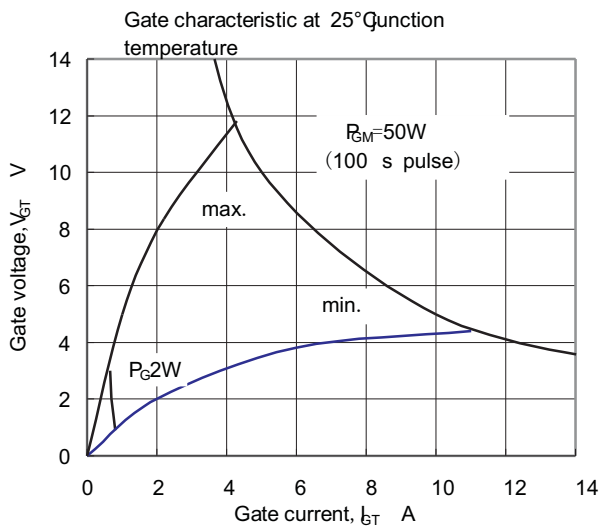


Fig. 9

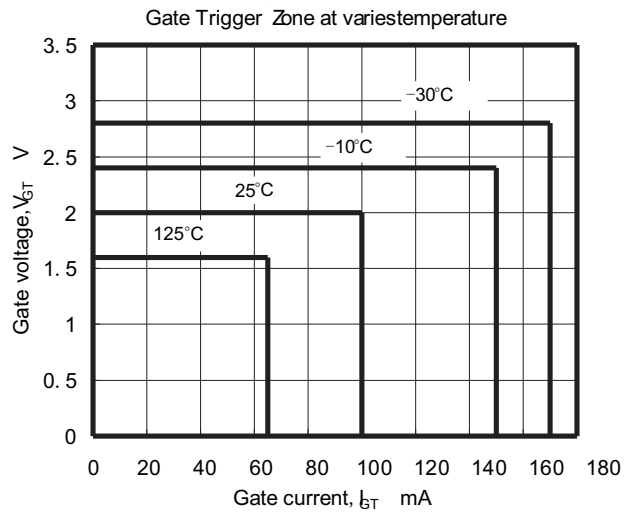


Fig. 10

